What is claimed is:

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1. A method for fabricating a contact pad of a semiconductor device, the method comprising:

forming a plurality of conductive layer patterns displaced on a silicon substrate with adjoining to each other;

forming an insulating layer on a top of the conductive layer patterns; depositing a material layer serving as a hard mask on the insulating layer; forming a photoresist pattern between the conductive layer patterns on the hard mask material layer to form a contact hole;

defining an area for forming a contact by forming by etching the hard mask material layer with utilizing the photoresist pattern as an etching mask;

removing the photoresist pattern;

exposing the silicon substrate by etching the insulating layer with utilizing the hard mask as an etching mask to thereby form an open portion;

forming a polymer layer on the open portion;

exposing the silicon substrate by removing the hard mask and the polymer layer by implementing an etch back process; and

forming a contacted pad on the exposed silicon substrate.

- 20 2. The method of claim 1, wherein the conductive layer pattern includes any one of a gate electrode pattern, a bit line pattern or a metal wiring.
 - 3. The method of claim 1, wherein, in the step of forming the photoresist pattern comprises using an argon fluoride (ArF) photoresist and an ArF light source.

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- 4. The method of claim 1, wherein the hard mask material layer includes an insulating material layer selected from the group consisting of a SiC layer, an undoped poly silicon layer, a silicon nitride layer, and a silicon oxide nitride layer.
- The method of claim 1, wherein the insulating material layer is formed at a thickness ranging of about 400 Å to about 2000 Å.

a conductive material layer selected from the group consisting of a tungsten layer, a tungsten silicide layer or a doped poly silicon layer. 5 7. The method of claim 1, further comprising the step of forming a bottom arc layer with an organic material. 8. The method of claim 1, wherein the contact pad is a doped poly silicon layer. 10 9. A semiconductor device made in accordance with the method of claim 1. 10. A semiconductor device made in accordance with the method of claim 2. 15 11. A semiconductor device made in accordance with the method of claim 3. 20 12. A semiconductor device made in accordance with the method of claim 4. 13. A semiconductor device made in accordance with the method of claim 5. 25 14. A semiconductor device made in accordance with the method of claim 6. 15. A semiconductor device made in accordance with the method of claim 30 7. 16. A semiconductor device made in accordance with the method of claim 8.

The method of claim 1, wherein the hard mask material layer includes

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